ANALYSIS OF GATE-ALL-AROUND STACKED NANOSHEET THIN FILM TRANSISTORS (GAA SNSTFT) FOR LOW POWER APPLICATIONS

A SYNOPSIS

Submitted by

JENYFAL SAMPSON

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(DEEMED TO BE UNIVERSITY)

ANAND NAGAR, KRISHNANKOIL - 626126

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1. INTRODUCTION

When the gate's control of the channel region is influenced by electric field lines from the source and drain, short-channel effects occur. The electric field lines propagate across the depletion zones associated with the junctions in a bulk device. By raising the doping concentration in the channel region, their influence on the channel can be decreased. Unfortunately, the doping concentration in very small devices (10^{19} cm^{-3}) becomes too high for proper device operation. As transistor dimensions shrink, the close proximity of the source and drain decreases the gate electrode's capacity to control the potential distribution and current flow in the channel region, and undesired effects known as "short-channel effects" begin to plague MOSFETs. For all practical purposes, scaling the size of traditional “bulk” MOSFETs below 20nm appears to be unachievable.

Silicon-on-insulator MOS transistors have progressed from traditional, planar, single-gate devices to three-dimensional devices with a multi-gate structure in an ongoing effort to enhance current drive and better regulate short channel effects (double-, triple- or quadruple- gate devices). SOS (Silicon-On-Sapphire) devices were succeeded by partially depleted silicon MOSFETs (PDSOI). PDSOI MOSFETs were originally developed for specialized applications such as radiation-hardened or high-temperature circuits. As major semiconductor manufacturers began to adopt PDSOI technology to create high-performance microprocessors around the turn of the century, it became widespread. By making contact between the gate electrode and the floating body of the device, the low-voltage performance of PDSOI devices can be improved. The subthreshold slope, body factor, and current drive are all improved, however the device can only operate at sub-1V supply voltages. The electrostatic coupling between the gate and the channel is better in fully depleted SOI (FDSOI) devices. As a result, the linearity, subthreshold slope, body coefficient, and current drive are all improved. FDSOI technology is employed in a variety of applications, including low-voltage, low-power integrated circuits and radio frequency integrated circuits.

Sandwiching a fully depleted SOI device between two gate electrodes connected together can significantly reduce short-channel effects. Because the device's cross section resembles the Greek letter Ξ, it was given the name XMOS (Xi). The channel depletion region is more controlled in this design than in a “regular” SOI MOSFET, and the influence of the drain electric field on the channel is reduced, which

lowers short-channel. The hard mask in the FinFET structure prevents parasitic inversion channels from forming at the device's top corners.

A thin-film, narrow silicon island with a gate on three sides is known as a triple-gate MOSFET. By extending the sidewall parts of the gate electrode to a depth in the buried oxide and underneath the channel region, the electrostatic integrity of triple-gate MOSFETs can be improved. The surrounding-gate MOSFET is the structure that theoretically allows the best possible control of the channel region by the gate, and thus the best possible Electrostatic Integrity. Because the silicon island was significantly broader than thick, the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region. The GAA abbreviation is now commonly used to refer to quadruple-gate or surrounding-gate devices with a width-to-height ratio much closer to unity. Multiple channels can be built on top of one another to improve current drive per unit area while sharing a common gate, source, and drain. MOSFETs with several bridge channels are known as Multi-Bridge Channel MOSFETs (MBCFET).

TiN, TiSiN, TaN, and TaCN are metal nitrides that are stable at extremely high temperatures. After high-temperature annealing, the work functions of these metals are typically between 4.4eV and 4.7eV, depending on: 1) layer thickness, 2) alloy composition, 3) crystal orientation, and 4) gate dielectric material. Metal nitrides aren't good gate materials for planar CMOS, but they have the correct work function for low-power, multi-gate CMOS applications, hence they've been used to make multi-gate MOSFETs. The device's current drive can be improved further by using strained silicon, a metal gate, and/or a high-k dielectric as the gate insulator.

The metal work function, the semiconductor's energy bandgap, electron affinity, and work function all influence the electrostatic state at the MS contact, which effects band alignment. The electrostatic characteristics near the interface are also influenced by the applied electric field, if any.

2. LITERATURE REVIEW

The International Technology Roadmap for Semiconductors (ITRS) 2015 shows that the GAA NWFET design is much more suitable for Nano level devices. The GAA NWFET structure is more feasible since the gate takes complete control over the channel and reduces short channel effects by Colinge [1]. Different shapes of Nanowire

are given in Alameri et al. [2], and among them, the cylindrical structure provides better performance than other structures. After the MOSFET revolution, there were many methods and structures introduced to increase the performance of the device when the device length is narrowed down. The MBCFET concept was introduced to increase the current in MOSFET. Due to the incorporation of multiple channels in the device, the width was increased. As a result of which the current drive was also increased. The first MBCFET model was fabricated in 2003 for a channel length of 5 μm and showed that this device could increase the output current, reported by Lee et al. [3]. Following that, an MBCFET with a gate length of 250nm was fabricated in Lee et al. [4]. Fabrication of MBCFET with sub 30 nm gate length has been explained in Yoon et al. [5]. Based on the number of channels that have been divided from a single channel, the MBCFET assures high current drivability. Silicon Carbide (SiC) was experimentally proven and introduced as a source and drain material, which induced horizontal tensile strain and vertical compressive strain in the Silicon (Si) channel region, thus increasing 50% of the current drive for a gate length of 50 nm, reported by Ang et al. [6].

In recent years, researchers have focused on utilizing the benefits of a junction less (JL) thin film transistor device due to its ease in fabrication and lower thermal budget issues than regular devices. The first JL nanowire transistor was made in 2010 by Colinge et al. [7]. The gate region is formed with two metals having different work functions. The difference in work functions of metals causes the potential step to change near the junction, as a result of which the carrier velocity, carrier transport efficiency and drain current are increased, reported by Pal and Sarkar [8]. The work function of Titanium Nitride (TiN) metal gate can be tuned by varying the thickness of the TiN layer. The cost of fabrication for each metal gate can be reduced. Kang et al. [9] and Hasan [10] discuss the tuning of the work function using TiN and titanium silicon nitride (TiSiN) for FinFET and FDSOI transistors. The work function increases with increasing nitrogen content.

In Pravin et al. [11], by building DMGs in cylindrical nanowires and analyzing with various gate oxides, the superiority of HfO_2 dielectric over other oxide layers has been established. Similar manner, Double gate transistor has been analyzed with various gate oxides in Thriveni and Ghosh [12]. Inverter and SRAM circuits have been built and analyzed in Pravin et al. [13] and Pravin et al. [14] by using cylindrical structure transistor.

3. RESEARCH PROBLEM

As previously mentioned, the large current drive in FinFET's can be achieved to an extent but with sufficient trade-off in the die area. Appropriate materials are required to implement gate regions all over the device to ensure proper functionality of the device.

1. A stacked nanosheet can be implemented in a thin film transistor but it gets prone to high leakage in the subthreshold condition. This weakens the device.
2. The controllability of the device needs to be enhanced at the gate region. Although large current drives are produced, a better I_{ON}/I_{OFF} ratio is required to efficiently control the carrier transport in the gate region.
3. The feasibility for fabricating multi-material-based Gates is thin due to presence of different metal work functions. Also, this device needs to be appropriate for developing smaller circuits before it can be proved for low power applications.

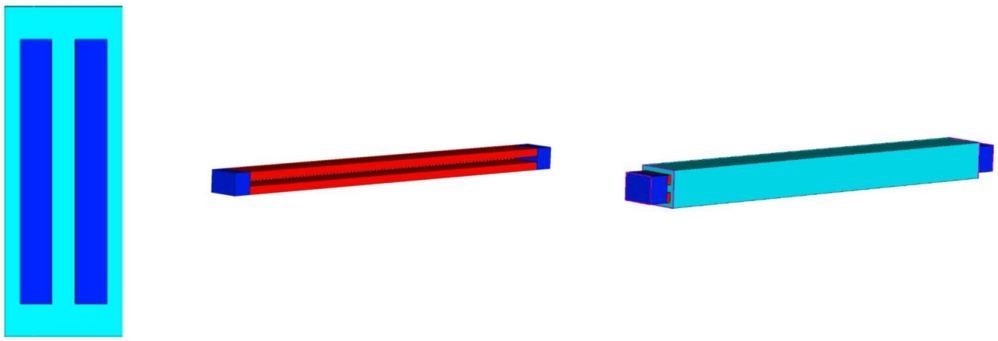
4. OBJECTIVES OF THE WORK

The main objectives of this research work are:

1. To use dielectric engineering by testing several dielectric materials in stacked nanosheet device to reduce the leakage current and better performances.
2. To improve the controllability at the gate region of the GAA SNSTFT device by incorporating triple material gate regions with distinct work functions. The I_{ON}/I_{OFF} ratio can further be enhanced that determines better carrier transport in the region.
3. By forming a p-type Metal, Titanium Nitrate (TiN) having its Work function in the Mid-gap region will be used. I_{ON} current of the order of 20μA needs to be achieved. Also, the testing of the device's appropriateness for developing smaller circuits before it can be proved for low power applications.

5. OVERVIEW OF THE SEGMENTED RESULTS

The structure of the device in the Figure 1(a), (b) and (c) which has been modelled with the TCAD tool with the details given in the Table 1. The work function is 4.725 and has been used for the simulation followed by the direct metal gate which has been given as a contact. The structure modelled in has been formed using SiO2.



(a) (b) (c)

Figure 1(a) Oxide Layer around channels, (b) Stacked Nanosheets without oxide layer, (c) Gate All Around Stacked Nano sheet

Table 1 Parameters used in GAA SNSTFT

SI. No.	Parameters	Values (unit)
1	Gate length, L_G	1000 (nm)
2	Channel fin width, F_W	80 (nm)
3	Top channel fin height, F_{ht}	20 (nm)
4	Bottom channel fin height, F_{hb}	20 (nm)
5	Interlayer oxide	15 (nm)
6	Gate oxide	10 (nm)
7	S/D doping (Boron)	$1x10^{20}$ (nm)
8	Channel doping (Phosphorous)	$1x10^{16}$ (nm)

Figure 2, illustrates the schematic view of the p-channel SM SNS GAATFT which is formed using the TCAD Simulation tool from the parameters that have been taken from experimental work.

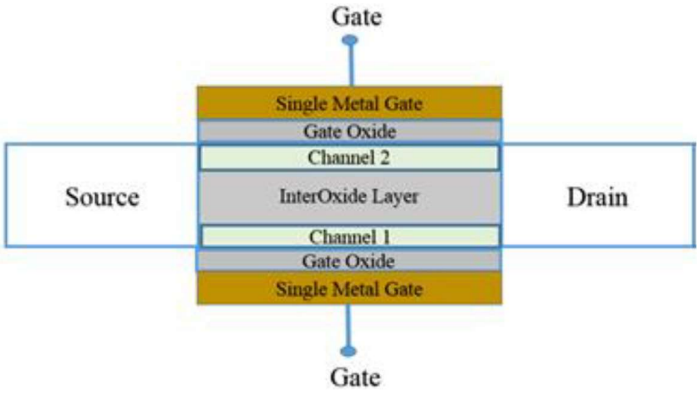
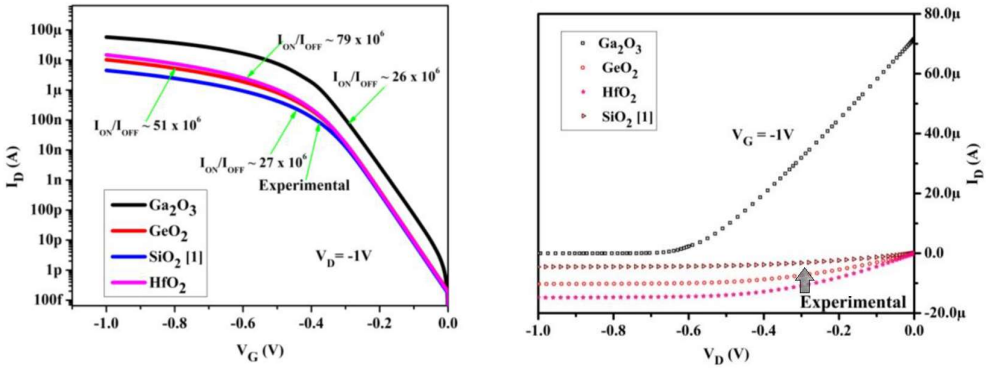


Figure 2 Schematic view of a SM SNS GAATFT

The IV Characteristics have been measured for the device (SNS GAATFT) having taken the values of VGS= -1V and VDS = -1V with different materials like SiO2, Ga2O3, HfO2, GeO2. As seen in Figure 3(a), transfer characteristics clearly shows the better performance of the material among them, based on the I_{ON}/I_{OFF} calculation.

In Figure 3(b), the output characteristics have been made for the same device with different materials. Based on the output results, High-k dielectrics increased the performance of the Thin Film Transistor and simultaneously Gate all around structure reduces the leakage current and short channel effects which can apply for AMOLED applications.



(a) (b)

Figure 3 (a) Transfer Characteristics and (b) Output Characteristics of Gate All Around Stacked Nanosheet with different dielectric material.

Table 2 shows calculated threshold and Subthreshold Swing (SS) values for different dielectric materials in the same SNS GAATFT. Comparing SS values with different dielectric materials, almost ideal value has got in all materials when TFT is used with stacked Nano sheets.

Table 2 Threshold and SS values for different dielectric materials

OXIDE MATERIAL	***THERSHOLD VOLTAGE (V)***	***SS (mV / dec)***
Ga_2O_3	-0.29	61
HfO_2	-0.36	61
GeO_2	-0.35	61

In Figure 4, the SM gate is replaced by the TM gate, i.e. it is a TM SNS GAATFT. From the structure it is seen that the gate electrode consists of three different WFs (φ) based materials M1, M2 and M3 that are deposited over the lengths L1, L2 and L3, respectively, on the gate oxide layers. ϕM1, ϕM2, ϕM3 are the material WFs for the first, second and third gate, respectively, and it is chosen that ϕM1 < ϕM2 < ϕM3 is the consideration for the p-channel transistor. The total length of the metal is L = L1 + L2 + L3, each having the same length of 333 nm.

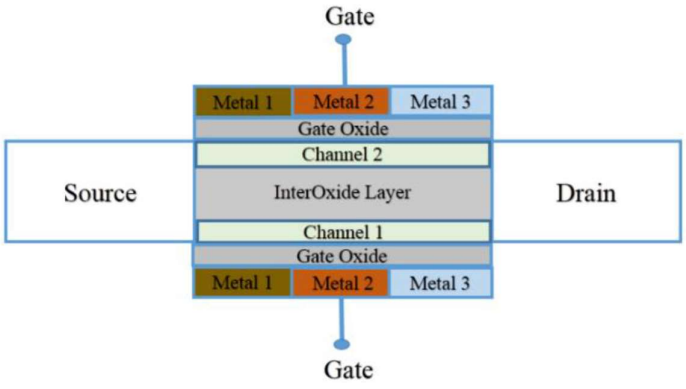


Figure 4 Schematic view of the proposed TM SNS GAATFT

Figure 5 depicts the comparison of electric potentials of the SM gate (SMG) and TM gate (TMG). The values of V_G = – 0.3 V and V_D = – 0.5 V are considered for operation. In the SMG, it is noticed that the electric potential monotonically increases from the source to the drain, whereas there is an abrupt change near the transition of different gate materials in the TMG.

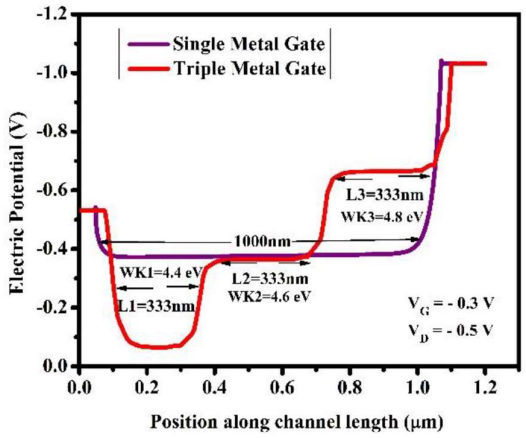
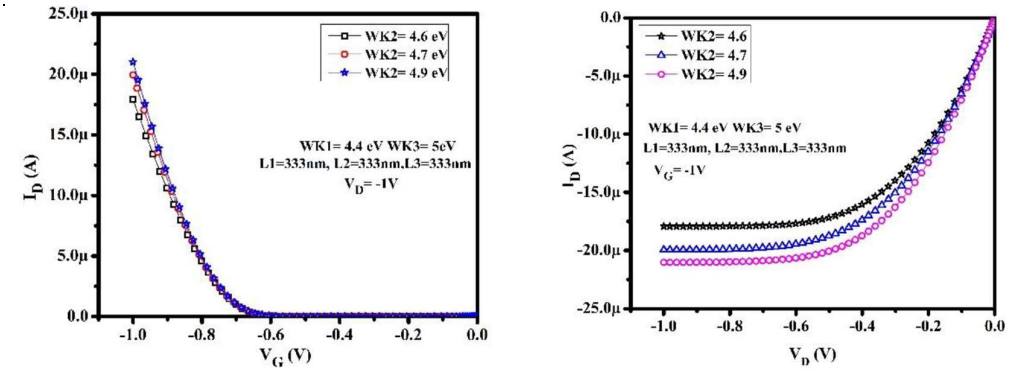


Figure 5: Electric potential variation for different channel lengths (μm) across the proposed TM and SM.

Figure 6(a), shows the output characteristics of the proposed TM model. The *p*-channel based transistor is applied with constant WFs WK1 and WK3 while varying WK2 from lower to higher value. The voltage is equal to the supply voltage *VDD*, i.e., $V_G = -1$ V is applied on the gate terminal to observe the on-current (I_{ON}) of the transistor. It is observed that with the maximum WF of 4.9 eV, a higher I_{ON} of 22 µA is obtained in comparison to 7.5 µA at 4.6 eV.

Figure 6(b), depicts the transfer characteristics of the p-channel transistor varying work function WK2 having constant $V_D = -1$ V. The characteristics obtained prove the behaviour of a MOSFET, and little variation in the threshold voltage (V_T) in the saturation region can be observed. The maximum saturation current of 20 µA is also obtained as in the case of the output characteristics.



(a) (b)

Figure 6: (a) Transfer characteristics of the proposed TM model by varying WF of WK2 keeping WK1 and WK3 constant at a constant $V_D = -1$V, (b) Output characteristics of the proposed TM model by varying WF of WK2 keeping WK1 and WK3 constant at a constant $V_G = -1$V.

Figure 7 shows the comparison of the output currents of a SM SNS GAATFT with respect to that of a TM SNS GAATFT. From the previous results for the M2, WK2 = 4.9 eV is being used due to higher I_{ON} current. As specified earlier, in the p-channel device the second screen gate (M3) has a higher WF compared to that of M1. We can thus infer from the comparison that the drain current in the TM is almost 4 times higher than that of the SM model.

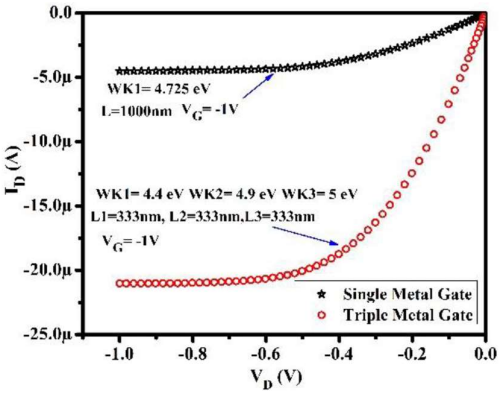


Figure 7: Comparison of drain currents of SMG and TMG with respect to varying drain voltage.

For the third work, the proposed structure Figure 1 with the Poly Silicon Gate material has been replaced with a TiN Metal gate, and analyzed using HfO_2 and SiO_2 as dielectric materials.

The same system structure is simulated with TiN metal gate where the IV characteristics has been matched with the experimental results. TiN Metal gate gives better performance than Poly Silicon with SiO2 as the oxide material, as shown in Figure 8.

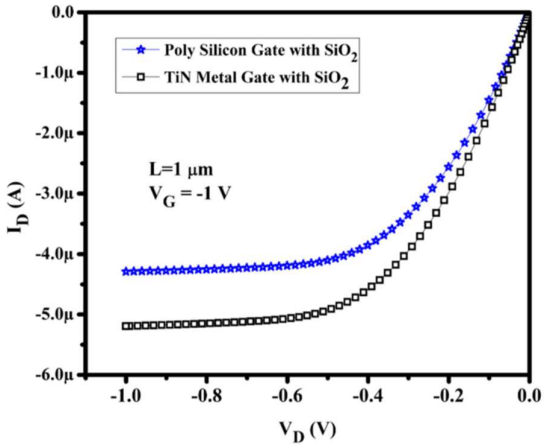


Figure 8: Experimentally derived output characteristics of GAASNSTFT with SiO_2 dielectric with polysilicon metal gate compared with TiN Metal gated device.

Figure 9 shows the Channel formation, that is well controlled by the surrounding Gate with varying Electrostatic Potential (V). It displays potential variation in the two channel regions. The two oxide regions around the channels have been removed to better view and understand how the electrostatic potential varies along the channel length region.

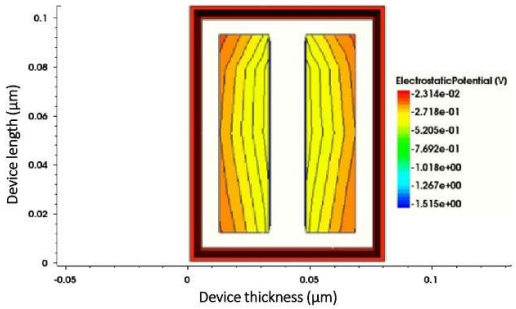


Figure 9: SNS controlled by influence of GAA structure.

When TiN thickness decreases from 20 to 2 nm, the potential increases as shown in Figure 10, which proves the tuning of the work function in the meV range.

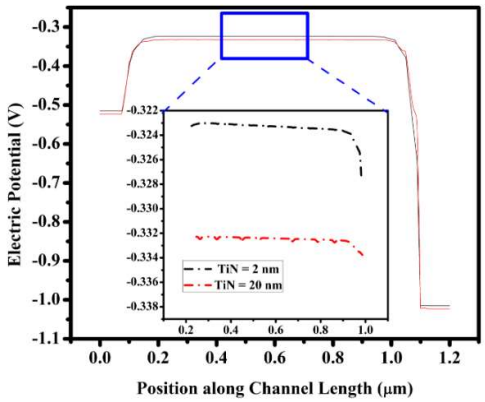
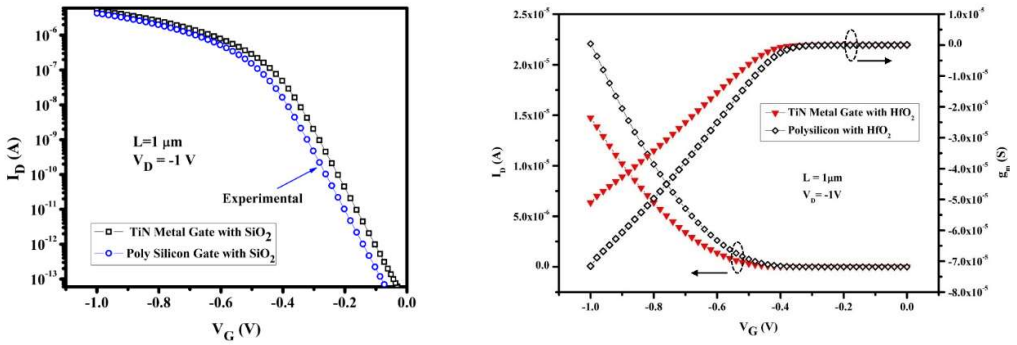


Figure 10: Electric potential variation of the proposed GAASNSTFT with different TiN thickness.

Figure 11(a) shows the transfer characteristics of the TiN metal gate when using SiO_2 as a dielectric. It is compared with an experimental result from [15] that used a Polysilicon gate with SiO_2 material. The drain voltage is kept constant at -1 V, and the gate bias is swept from 0 to -1 V. This analysis has been carried out for both SiO_2 as well as HfO_2 oxides. In doing so, HfO_2 has given better performance, compared to SiO2. Thus, instead of using SiO_2, the TiN and Poly Silicon materials have been analysed with HfO_2 in the subsequent analysis and the result has been illustrated in Figure 11(b). TiN shows an impressive performance in comparison to the Polysilicon device.

In the drain current perspective, the proposed TiN-gated device with HfO_2 dielectric has provided around 5 times better performance compared to the Poly Silicon-gated device with SiO_2 dielectric.



(a) (b)

Figure 11: Comparison of the Transfer Characteristics of the GAASNSTFT (a) with SiO_2 dielectric considering TiN and Poly Silicon as Metal gate, (b) with HfO_2 dielectric considering TiN and Poly Silicon as Metal gate.

The proposed structure's output characteristics with varying thickness is plotted in Figure 12. Here the calibration is performed at three different TiN thickness values: 1.5, 8 and 18 nm, and has been found that there is an ignorable change in drain current by varying the thickness, which is due to the tuning of the work function. When V_G is equalled to VDD and larger than the threshold voltage (V_{th}), i.e., V_G = VDD > Vth, the electron inversion layer will appear, and nFET will be conducting. On the other hand, the source and body of pFET are connected to VDD, thus the applied V_G is just the opposite of nFET. When V_G = VDD, the nFET is conducting and pFET is OFF. On the contrary, when V_G = 0, nFET is OFF and pFET is conducting.

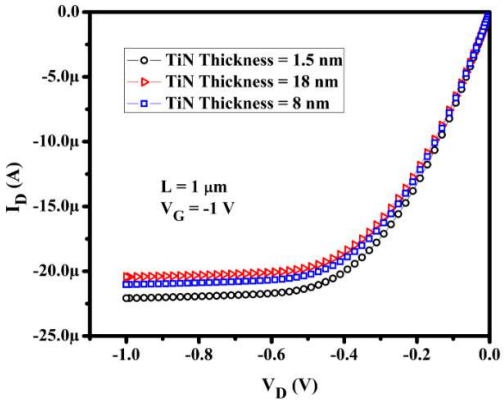
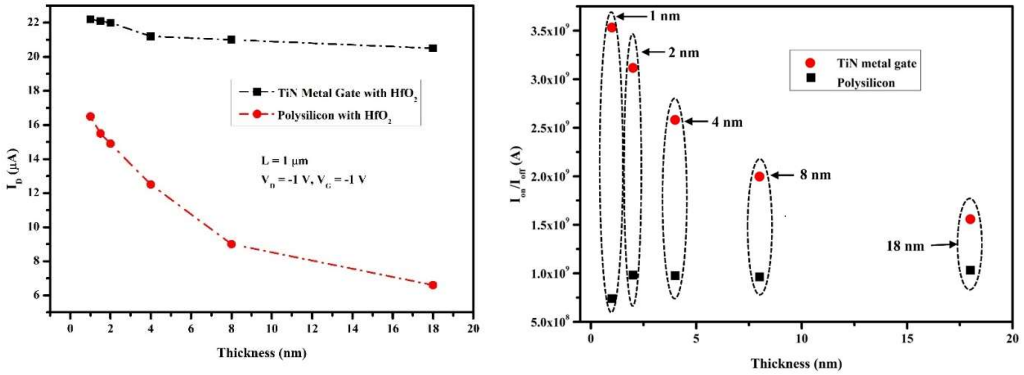


Figure 12: Comparison of the Output Characteristics of the proposed GAASNSTFT with different TiN thickness.

To predict the saturated value of work function modulation, the thickness of the TiN is varied from 18 nm to a minimal value. In Figure 13(a) its shown that below 1.5 nm TiN thickness, the I_D gets saturated. Due to an effective nitrogen content in the TiN metal contact, the current gets saturated below 1.5 nm thickness. TiN is oxidized and becomes nitrogen deficient when thickness is high. Figure 13(b) shows a comparison of I_{ON}/I_{OFF} ratio of the proposed structure at various metal layer thicknesses when compared to polysilicon device.



(a) (b)

Figure 13: (a) Saturated value prediction of Work Function Modulation by varying the TiN thickness values, (b) I_{ON}/I_{OFF} ratios of the proposed TiN metal gate GAA SNSTFT compared with that of polysilicon TFT for various metal gate thickness values.

The proposed GAA SNSTFT structure's inverter for circuit level simulation has been developed using Sentaurus TCAD, and a schematic illustration has been shown in Figure 14.

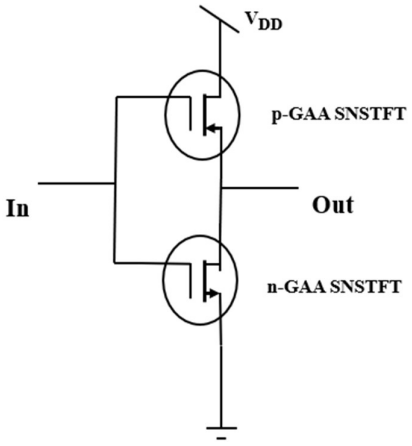
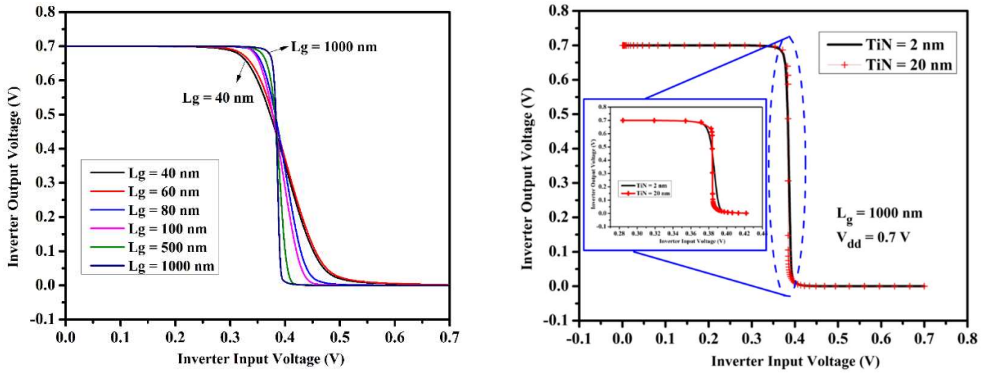


Figure 14: Inverter Circuit built using the proposed GAA SNSTFT.

The Voltage Transfer Characteristics (VTC) for the inverter has been calibrated with different channel lengths as shown in Figure 15(a). It has been implied that the inverter functions properly for gate lengths upto 80 nm, and lower lengths will be highly vulnerable to SCE. A comparison of the VTC curves yielded for 2 and 20 nm TiN thicknesses has been shown in Figure 15(b). There is a 5% and 12% improvement in NMH and NML respectively, for a TiN thickness of 2 nm in comparison to that of 20 nm.


Inverter Output Voltage (V)
Inverter Input Voltage (V)
Lg = 1000 nm
Lg = 40 nm
Lg = 40 nm
Lg = 60 nm
Lg = 80 nm
Lg = 100 nm
Lg = 500 nm
Lg = 1000 nm
TiN = 2 nm
TiN = 20 nm
Lg = 1000 nm
Vdd = 0.7 V

(a) (b)

Figure 15: Comparison of Voltage Transfer characteristics of an Inverter for the proposed GAASNSTFT

(a) using different channel lengths, (b) for varying TiN thickness using Lg = 1000nm.

Calibrating the device at low gate lengths produces higher subthreshold swing with decreasing threshold voltage. A short description of the performance of several short channel effects like subthreshold swing and threshold voltage roll-off for various channel lengths has been demonstrated in the Table 3.

Table 3: Comparison of SCE such as SS, threshold voltage roll-off and DIBL with various channel lengths.

Channel length (nm)	***Subthreshold swing (mV/dec)***	***Threshold voltage roll-off (V)***
80	58	-0.056
60	61	-0.135
40	101.26	-3.587
20	152.78	-5.289

Table 4 compares the noise margin values produced by different oxide materials for the circuit. V_{NMH} is high in SiO_2, but V_{NML} is relatively low. The results show that HfO_2 will be well suitable for building GAA, Multi-Bridge Channel (MBC) structures and other sub-10 nm devices, proving that it is a good substitute for SiO_2.

Table 4: Noise margin values for different oxides.

Oxide material	***V_{NMH} (V)***	***V_{NML} (V)***
SiO_2	0.21	0.06
HfO_2	0.16	0.22

The schematic illustration of a 6 T SRAM designed using the proposed GAA SNSTFT is shown in Figure 16. It has been developed in a similar manner to that of Inverter using Sentaurus TCAD.

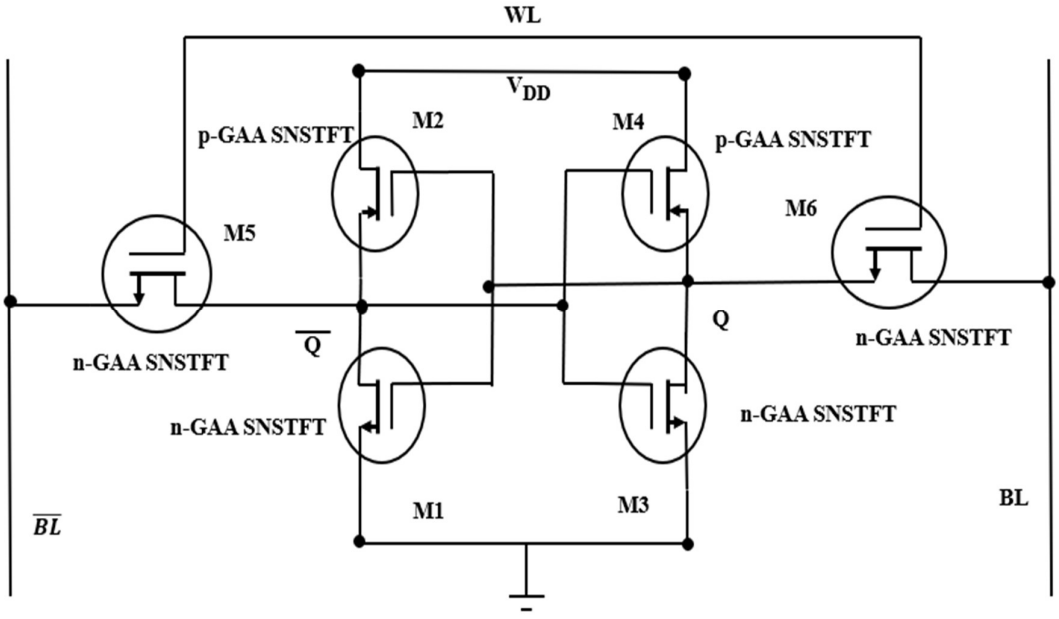
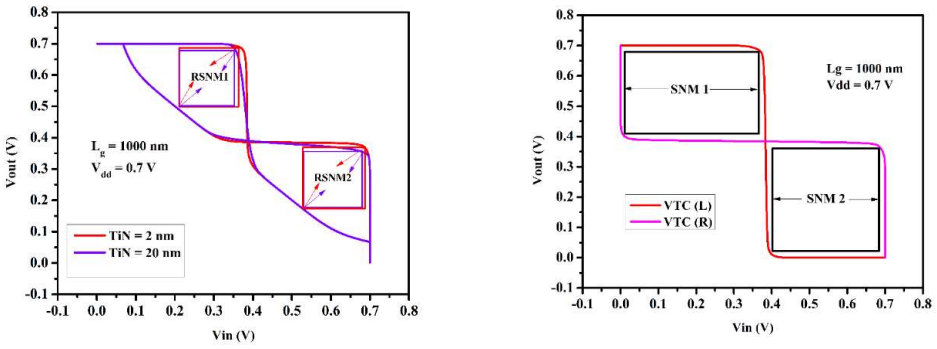


Figure 16: 6T SRAM Circuit built using the proposed GAA SNSTFT.

Figures 17(a) and 17(b), show the Read and Hold butterfly diagram of the proposed GAASNSTFT for TiN thicknesses of 2 and 20 nm. A gate length of 1 μm is used as it provides better results as seen in the Inverter circuit above. An input voltage (VDD) of 0.7 V is given for the circuit.



(a) (b)

Figure 17: (a) Read Butterfly diagram, (b) Hold Butterfly diagram of 6T SRAM with TiN based GAASNSTFT

Table 5 represents the signal to noise ratios of the first and second signals for read, write and hold states, derived using the butterfly diagram. A 14% increase is obtained in the RSNM while using a TiN thickness of 2 nm compared to 20 nm.

Table 5: Estimation of 6T SRAM performance for various TiN thickness of GAASNSTFT.

TiN thickness	***Read***		***Write***		***Hold***	
	SNM1	**SNM2**	**SNM1**	**SNM2**	**SNM1**	**SNM2**
2 nm	0.16	0.16	0.059	0.316	0.35	0.289
20 nm	0.14	0.15	0.051	0.312	0.35	0.282

The delay estimation of the proposed 6 T-SRAM has been represented in Table 6, compared with other SRAM terminologies. The proposed 6 T-SRAM structure using GAA SNSTFT yielded 65.34 ps read and 7.36 ps write delays, thus proving to be comparatively time efficient than most other SRAM cells.

Table 6: Delay performance of the proposed GAA SNSTFT-based 6T-SRAM compared with other SRAM terminologies from literature.

SRAM Cell	***Number of transistors***	***Delay (ps)***	
		Read	**Write**
12T	12 (2 PMOS and 10 NMOS)	69.34	981.274
10T	10 (2 PMOS and 8 NMOS)	29.38	1.73
8T	8 (2 PMOS and 6 NMOS)	77.72	45.47
6T	6 (2 PMOS and 4 NMOS)	72.82	8.976
4T	4 (2 PMOS and 2 NMOS)	1990	87.6
6T (proposed)	6 (2 PMOS and 4 NMOS)	65.34	7.36

6. ORGANIZATION OF THE THESIS

The structure of this thesis is organized into eight chapters, as follows:

Chapter 1

This chapter describes the motivation behind the use of Multi-channel transistor in place of Single Channel transistor, and the future developments in Multi-channel based Thin Film Transistor (TFT). The benefits of work function tuning of Gate material have been well analyzed in this section.

Chapter 2

A review on the various works carried out by researchers across multi-channel transistors and multiple material gate-based transistors devices have been reported in this chapter. Through the different structures and their characteristics, the motivation behind the proposed structure has also been defined here.

Chapter 3

This chapter talks about implementing the multi-channel structure in cylindrical device and thus varying the dielectric material of the oxide layer to increase the drain current value. The behavior of various parameters such as drain current, I_{ON} /I_{OFF} ratio and subthreshold swing of the device have been computed by Sentaurus TCAD.

Chapter 4

This chapter reports on the analysis of the Triple Material (TM) Gate SNS TFT. The TM of the TFT is varied by applying three different work functions (WFs) by having different gate materials being used. The analysis of varying WF2 by keeping WF1 and WF3 constant is done to prove that WF2 value closer to WF3 provides better results. Drain current up to 4 times larger than that of Single Metal has been obtained by simulating the results using Sentaurus TCAD.

Chapter 5

This chapter involves the analysis of tuning the Work function of a single Gate material and also making sure that the same drain current is obtained as in the previous work. The DC characteristics of drain current and I_{ON}/I_{OFF} ratio has been reported. Circuit analysis like Inverter and SRAM have been implemented and Voltage Transfer Characteristics and Static Noise Margin also reported.

Chapter 6

This chapter draws a conclusion to the thesis, and also discusses the future work to be carried out in this context.

7. CONCLUSION

In the first work the SNS GAATFT is formed with different dielectric materials and I_{ON} / I_{OFF} have been analysed. TFT with GAA structure reduces SCE and increased the performance of the device. In future we believe that SNS GAATFT will create more impact in ultra-low power applications.

In the work that follows, the simulation and performance analysis in terms of electric potential of a TM SNS GAATFT has been carried out in comparison to a SM SNS GAATFT. In the study, results prove to have better I_{ON} / I_{OFF} ratio which makes it suitable for low power applications like OLED displays.

In the final work, an optimization of device performances for a GAA SNSTFT formed using TiN as the metal gate and analysed using both SiO_2 and HfO_2 as dielectric materials. Two channels are stacked in the design model. Both of the channel areas where TiN has been used to evaluate the electrostatic potential change have stronger gate controllability. By varying the TiN thickness, the work function has been tuned and the saturated value has been predicted. The proposed structure attains a high drain current of 22.5 μA, that is about 40–45% higher than the one obtained through polysilicon contact in the conventional structure. Moreover, the designed GAA SNSTFT device has been developed into inverter and 6 T-SRAM circuits, and their corresponding VTC characteristics has been evaluated for different channel lengths and TiN thicknesses. As opposed to an n-channel device where the noise increases with TiN thickness reduction and channel length increase, here for the p-channel device, a reduction in noise was observed while increasing channel length to 1 μm, simultaneously while decreasing the thickness of TiN. This device yielded a good amount of current drive compared to other conventional TFT stacked nanosheets, while reducing the leakage current due to the presence of GAA structure. The TiN metal gate functionality for the proposed GAA SNSTFT has also brought about enhanced controllability in-terms of I_{ON} / I_{OFF} from the inverter and static noise margin levels from the SRAM model. With a comparably lower gate length (1 μm), this device can be a suitable alternate for AMOLED pixel circuits, which will be carried out in the future.

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LIST OF PUBLICATIONS

1. Sampson, J., Siva Kumar, P., Velmurugan, S.P., “Analysis of GAA SNTFT with Different Dielectric Materials”, ICDCS 2020 - 2020 5th International Conference on Devices, Circuits and Systems, 2020, pp. 283–285, 9075738.
2. Sampson, J., Sivakumar, P., Velmurugan, S.P., “Simulation and Performance Analysis of a Triple-material Gate GAA SNSTFT”, Journal of Nano- and Electronic Physics, 2020, 12(6), 06006.
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